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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,493	12/11/2003	Yew Wee Cheong	42P17612	1630

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EXAMINER	
MCNALLY, DANIEL	

ART UNIT	PAPER NUMBER
1733	

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06/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,493	CHEONG ET AL.	
	Examiner	Art Unit	
	Daniel McNally	1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in response to the Amendment filed 4/23/2007.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1, 4, 5 and 24 are rejected under 35 U.S.C. 102(a) as being anticipated by Kumamoto [US2003/0001283] (of record, previously cited).

Kumamoto discloses a method of producing a chip assembly. The method comprises applying a coating (550/550') to a wafer (110), covering bumps (130) or "connection structures" (paragraph 0035). Note the disclosure of a backgrinding process (350) (paragraph 0039), and the dicing of the wafer (800) into dice (paragraph 0042). Kumamoto also discloses flipping a singulated die (800') together with its coating and connecting the die, with its coating in contact, to a substrate (960) (paragraphs 0042 and 0043), and the coating is located between the die and the substrate after the die is connected to the substrate, as seen in Figures 10 and 13.

With regard to claim 4, Kumamoto discloses a solder bumped wafer (paragraph 0022) comprising solder bumps (130) or "balls" as seen in Figure 1.

With regard to claim 5, Kumamoto discloses the application of heat to connect the bumps and the lands (970) by solder flow (paragraph 0043).

With regard to claim 24, Kumamoto discloses the surface of the wafer comprises a circuit surface (120) (paragraph 0022).

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 3, 6, 7 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamoto in view of Nguyen et al. [US6352881] (of record, previously cited).

Kumamoto discloses a method of producing a chip assembly. The method comprises applying a coating (550/550') to a wafer (110), covering bumps (130) or "connection structures" (paragraph 0035). Note the disclosure of a backgrinding process (350) (paragraph 0039), and the dicing of the wafer (800) into dice (paragraph 0042). Kumamoto also discloses flipping a singulated die (800') together with its coating and connecting the die, with its coating in contact, to a substrate (960) (paragraphs 0042 and 0043), and the coating is located between the die and the substrate after the die is connected to the substrate, as seen in Figures 10 and 13.

With regard to claims 6 and 23, Kumamoto discloses the coating as a thermoset polymer (paragraph 0036). Epoxy is a thermoset polymer, however Kumamoto is silent as to specifically using an epoxy.

With regard to claim 3 and 6, Kumamoto does not disclose partially curing the coating after application. In Figure 11, it can be determined that steps have been made to keep the coating from dripping off the die when the die and coating are flipped.

With regard to claim 7, Kumamoto discloses the application of heat to flow the solder bumps. Kumamoto does not disclose the heat also cures the coating.

Nguyen discloses a method of producing a flip chip assembly comprising a step of applying a layer of underfill adhesive (110) to a wafer (100) (column 3, lines 13-19). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47). Nguyen teaches a soft or pre-cure operation is performed to partially cure the underfill adhesive. Nguyen also teaches the application of heat causes the solder balls to flow and finally cure the underfill adhesive

It would have been obvious for one of ordinary skill in the art at the time of invention to use an epoxy based material in Kumamoto's coating as taught by Nguyen in order to have an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip, and to partially cure the coating of Kumamoto after application as taught by Nguyen in order to improve the handling of the wafer, and to finish curing the coating of Kumamoto as taught by Nguyen in order to create a strong bond between the die and substrate.

6. Claims 1,4,5 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamoto [US2003/0001283] (of record, previously cited) in view of Walsh [US3475867] (of record, previously cited).

Kumamoto discloses a method of producing a chip assembly. The method comprises applying a coating (550/550') to a wafer (110), covering bumps (130) or "connection structures" (paragraph 0035). Note the disclosure of a backgrinding process (350) (paragraph 0039), and the dicing of the wafer (800) into dice (paragraph 0042).

Kumamoto also discloses flipping a singulated die (800') together with its coating and connecting the die, with its coating in contact, to a substrate (960) (paragraphs 0042 and 0043), and the coating is located between the die and the substrate after the die is connected to the substrate, as seen in Figures 10 and 13. Kumamoto discloses applying an adhesive tape layer to the wafer before the grinding process in order to attach the wafer to a support surface during the grinding process, and removing the adhesive tape after the grinding process.

Walsh discloses a method of processing semiconductors. The method comprises spreading a wax coating on a carrier plate and depositing semiconductor wafers into the wax to mount the wafers on a carrier plate (column 7, lines 41-50). The mounted wafers then have a portion of the back surface of the wafer removed in a lapping machine (column 8, lines 35-55). After the wafers reach a desired thickness and are polished, the wafers are removed from the wax and carrier plate.

It would have been obvious to one of ordinary skill in the art at the time of invention to replace the adhesive tape of Kumamoto with wax to hold the wafer on a carrier plate during the backgrinding process as taught by Walsh in order to reduce the waste of the adhesive because the wax can be recycled and reused while the adhesive tape is good for only a single application.

With regard to claim 4, Kumamoto discloses a solder bumped wafer (paragraph 0022) comprising solder bumps (130) or "balls" as seen in Figure 1.

With regard to claim 5, Kumamoto discloses the application of heat to connect the bumps and the lands (970) by solder flow (paragraph 0043).

With regard to claim 24, Kumamoto discloses the surface of the wafer comprises a circuit surface (120) (paragraph 0022).

7. Claims 3,6,7 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamoto and Walsh and further in view of Nguyen et al. [US6352881] (of record, previously cited).

Kumamoto as modified discloses a method of producing a chip assembly. The applicant is referred to paragraph 6 above for a detailed discussion of Kumamoto as modified.

With regard to claims 6 and 23, Kumamoto discloses the coating as a thermoset polymer (paragraph 0036). Epoxy is a thermoset polymer, however Kumamoto is silent as to specifically using an epoxy.

With regard to claim 3 and 6, Kumamoto does not disclose partially curing the coating after application. In Figure 11, it can be determined that steps have been made to keep the coating from dripping off the die when the die and coating are flipped.

With regard to claim 7, Kumamoto discloses the application of heat to flow the solder bumps. Kumamoto does not disclose the heat also cures the coating.

Nguyen discloses a method of producing a flip chip assembly comprising a step of applying a layer of underfill adhesive (110) to a wafer (100) (column 3, lines 13-19). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47). Nguyen teaches a soft or pre-cure operation is performed to partially cure the underfill adhesive. Nguyen also teaches the application of heat causes the solder balls to flow and finally cure the underfill adhesive

It would have been obvious for one of ordinary skill in the art at the time of invention to use an epoxy based material in Kumamoto's coating as taught by Nguyen in order to have an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip, and to partially cure the coating of Kumamoto after application as taught by Nguyen in order to improve the handling of the wafer, and to finish curing the coating of Kumamoto as taught by Nguyen in order to create a strong bond between the die and substrate.

8. Claims 1,3-7, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh [US6338980] (of record, previously cited) in view of Nguyen [US6352881] (of record, previously cited) and Walsh [US3475867] (of record, previously cited).

Satoh discloses a method of forming a plurality of chips. The method comprises applying a protective resin to the active face of an IC wafer covering projected electrodes, grinding the inactive face of the IC wafer and dicing the wafer into a plurality of chips (column 3, lines 28-51). Satoh discloses in Figures 1D and 1E the step of dicing the wafer into a plurality of chips. The Figures further show as the wafer is diced, the protective coating is also cut into separate sections still attached to the wafer dice. Satoh discloses applying an adhesive tape layer to the wafer before the grinding process, removing the tape after the grinding process. Satoh also does not disclose attaching the chip to a substrate.

Walsh discloses a method of processing semiconductors. The method comprises spreading a wax coating on a carrier plate and depositing semiconductor wafers into the

wax to mount the wafers on a carrier plate (column 7, lines 41-50). The mounted wafers then have a portion of the back surface of the wafer removed in a lapping machine (column 8, lines 35-55). After the wafers reach a desired thickness and are polished, the wafers are removed from the wax and carrier plate.

Nguyen discloses a method of producing a flip chip assembly. Nguyen discloses aligning and mounting the flip chip onto a substrate so that the underfill is between the flip chip and the substrate (column 4, lines 30-38).

It would have been obvious to one of ordinary skill in the art at the time of invention to replace the adhesive tape of Satoh with wax to hold the wafer on a carrier plate during the back grind process as taught by Walsh in order to reduce the waste of the adhesive tape because the wax is reusable while the adhesive tape is only good for a single application, and to mount the chip on a substrate as taught by Nguyen in order to enable the chip to communicate with outside circuitry coupled to the substrate.

With regard to claim 4, Satoh discloses the projected electrodes as solder bumps (column 5, lines 41-46).

With regard to claim 5, Nguyen discloses applying heat to flow the solder balls (column 4, lines 30-38).

With regard to claims 3, 6 and 23, Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47), and that it is partially cured after application.

With regard to claim 7, Nguyen teaches applying heat to cause the solder bumps to flow and finally cure the underfill adhesive.

With regard to claim 24, Satoh discloses the wafer is a wafer having an IC surface.

Response to Arguments

9. Applicant's arguments filed 4/23/2007 have been fully considered but they are not persuasive. The applicant amended Claim 1 to remove new matter. The rejections in view of Kumamoto and Kumamoto in view of Nguyen have been reintroduced because they still read on the amended Claim 1. The rejections of the previous office action dated 1/23/2007 have been upheld. The applicant argues both Kumamoto and Satoh require the use of a peel away tape before mounting the die onto a package substrate. The applicant also argues Kumamoto and Satoh do not use the same layer as a protective layer and as underfill. With respect to Kumamoto, the removable adhesive layer adds to the protection of the wafer during backgrinding, however the coating layer (550/550') is considered the "protective layer" because the coating is in direct contact with the wafer and the circuitry on the wafer. This coating layer is also present as underfill when the wafer dice are bonded to a substrate. The examiner is not calling the removable adhesive layer the "protective/underfill layer." The teachings of Walsh have been included to show the removable adhesive layer does not have to be an adhesive, that other materials such as wax can be substituted for the removable adhesive. With respect to Satoh the protective resin is considered the protection during the backgrinding process and as the underfill when bonded to a substrate as taught by Nguyen. Satoh discloses using a temporary adhesive however the adhesive is not

considered the "protective/underfill layer" and the layer can be replaced by a wax as taught by Walsh.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel McNally whose telephone number is (571) 272-2685. The examiner can normally be reached on Monday - Friday 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel McNally
Examiner
Art Unit 1733

JEFF H. AFTERGUT
PRIMARY EXAMINER
GROUP 1300

/DPM/
June 7, 2007